Motor Control Specification

Analog control field parameters

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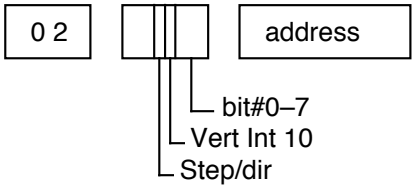
Motor control is specified via the contents of the analog control field of a given channel's analog descriptor. A number of cases are supported to handle various forms of motor I/O interfaces. This note describes the features available and how to specify them.

The form of the analog control field for a motor is as follows:



The analog control type byte is `$02` for motors. The values of the second byte provide for most of the variations. If the value of the byte is ≥ `$20`, then the last 3 bytes are interpreted as a pointer to a 1553 command block in the range `$200000` to `$EFFFF0` which can be used to send the two's complement count of motor steps to the hardware. In this case, the hardware is assumed to generate the pulses to step the motor automatically.

If the upper 3 bits of the second byte are zero, then we have the case of a memory-mapped digital I/O motor interface, and the local station cpu will arrange to deliver the motor steps pulses of about 20 μsec duration to the motor at 150 Hz. The rest of this note deals with variations of this memory-mapped case.

The least significant two bytes of the byte address used for motor control are given by the last two bytes of the field. The upper two bytes of the byte address are assumed to be `$FFFF` to indicate VME short I/O space in the local station crate. A variation of this is specified by bit#3 marked "Vert Int 10" above. If this bit is set, the upper two bytes are assumed to be `$10FF`, to indicate access to VME short I/O in a slave crate accessed via the Vertical Interconnect hardware. The slave crate is assumed connected to VI card#1, port#0. This feature allows testing Vertical Interconnect access.

Bit#4 is used to distinguish two types of hardware control of memory-mapped motor interfaces. When it is zero, the bit# indicates the CW pulse bit, and the adjacent bit (bit# exclusive-OR'ed with 1) indicates the CCW bit. For example, if the bit# given is 7, then the CW pulse is connected to bit#7 and the CCW pulse is run by bit#6.

When bit#4 of the second byte is a one, the bit# indicates the step pulse bit, and the adjacent bit is the direction control bit. Simultaneously, the bit# refers to the CW limit switch status, and the adjacent bit is the CCW limit switch status, where 1=limit switch active. This limit switch status byte is located either 1 or 2 bytes from the control byte, depending upon whether the address given is even (1) or odd (2). The Ironics digital I/O board is interfaced to odd bytes only, whereas the BurrBrown board is interfaced to consecutive bytes. To make this work with the latter board, motor control bytes should be connected to even byte addresses only.

To specify whether pulses should be low active or high active, the least significant bit of the bit# is used. If the given bit# is odd, high active pulses are issued. If it is even, then low active pulses are used. Since the bit also indicates which one is used for CW pulses (or for the step pulse), one cannot switch polarities independent of the hardware connections. So this factor must be considered when planning the wiring to the motor interface.

Summary

Several variations of motor control can be specified via proper settings of the analog control field. Motors can be controlled via 1553 interface, Ironics or BurrBrown digital I/O boards, CW/CCW or step/direction interfaces, hi-active or lo-active stepping pulses, and optional access via the Vertical Interconnect hardware to a slave VME crate. Providing more support variations than these may require a larger analog control field or indirect access via another table of specification parameters.